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2814

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Makoto Yamamoto

Serial No. 10/014,949

Filed: October 26, 2001

For: Lateral Transistor Having Graded Base Region,
Semiconductor Integrated Circuit And
Fabrication Method Thereof

) Art Unit: 2814

) Examiner: Shrinivas H. Rao

THIRD RESPONSE

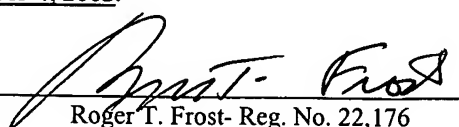
Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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TECHNOLOGY CENTER 2800

Responsive to the Office Action dated June 4, 2003 in the patent application identified above, please enter the following amendments and reconsider this application in view of the appended remarks.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 4, 2003.


Roger T. Frost- Reg. No. 22,176